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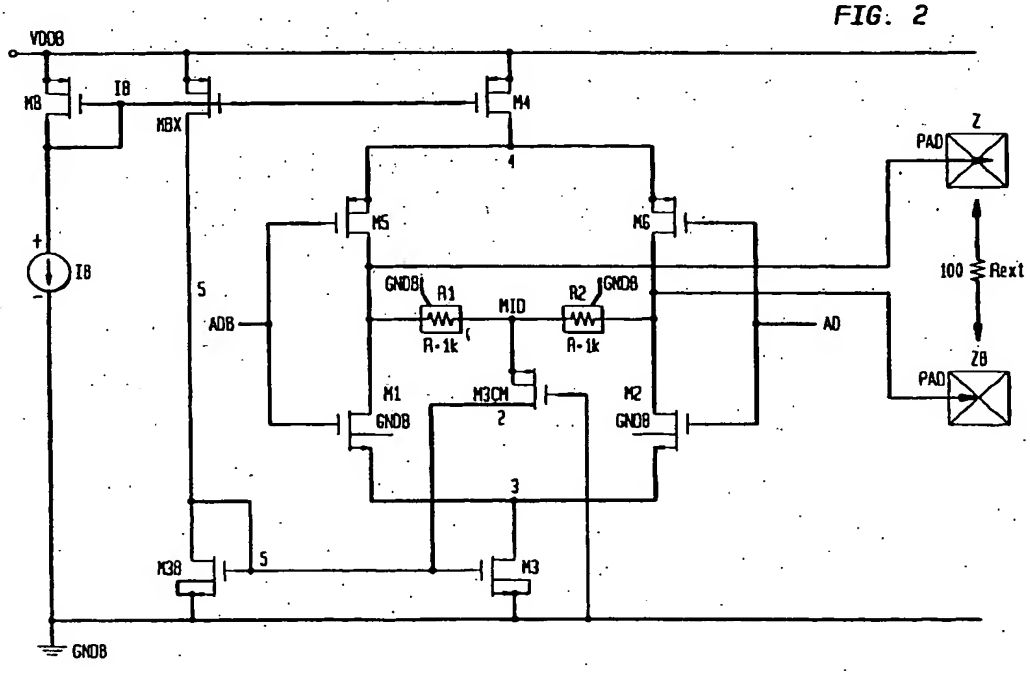
(54) Method and apparatus for controlling the common-mode output voltage of a differential buffer

(57) A method and device for controlling the common-mode output voltage of a differential buffer is disclosed. According to the invention, the common-mode output voltage of the differential buffer is controlled to a desired value by supplying a first current to the output of the differential buffer and supplying a second current to the output of the differential buffer, the second current being opposite in polarity and lower in magnitude than the first current. The common-mode output voltage of the differential buffer is sensed and an adjustment current is added to the second current to adjust the common-mode output voltage to the desired value.

FIG. 2



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Description

Field of the Invention

[0001] This invention relates generally to a method and apparatus for controlling the common-mode output voltage of a differential buffer, and is particularly useful for use with LVDS (Low Voltage Differential Signaling) output buffers.

Description of the Prior Art

[0002] A LVDS digital output buffer operates by changing the direction of current flow through circuitry placed between the buffers' two outputs (Z and ZB), in correspondence to the level of a digital input. The polarity of voltage developed across this circuitry is sensed by a receiver to recover the original digital level that was input to the buffer. To insure that the receiver functions properly, the common-mode output voltage of the buffer (the average value of the two outputs Z and ZB relative to ground) must be constrained to a specified range. A typical LVDS output buffer comprises a positive current source, negative current source, a means to switch the direction of current flow, and an operational amplifier (OPAMP) for setting the required output common-mode voltage.

[0003] The output common-mode voltage of a typical buffer can be controlled by varying the magnitude of the negative current source (alternatively called the tail current source). This is accomplished by an OPAMP based feedback loop controlling the tail current source magnitude. Figure 1 shows a prior art LVDS output buffer 10. The LVDS output buffer 10 has two outputs, Z and ZB. Internal resistor R1 and R2 of equal value, are placed in series between the outputs Z and ZB and sense, at node MID, the common-mode voltage of the outputs Z and ZB. The voltage at nodes Z and ZB, relative to MID, are equal in magnitude but of opposite polarity.

[0004] An external resistor R_{EXT} is placed across the nodes Z and ZB, and bias current source IB and transistors MB and M4 form a positive current source that sets up the current which will eventually flow through R_{EXT}. Transistors M1, M2, M5 and M6 switch the direction of current flow in R_{EXT} thereby changing the polarity of the voltage developed across R_{EXT} dependent upon the value of AD and ADB (ADB is always the inverted value of AD, e.g., if AD is a digital 1, ADB will be a digital 0, and vice versa). The amount of current flowing in transistor M3 (the tail current source) determines, i.e., controls, the common-mode voltage of the outputs Z and ZB.

[0005] To control the current in transistor M3 and thereby control the output common-mode voltage, an OPAMP based feedback loop is used to compare the common-mode voltage (V_{MID}) at node MID to a desired common-mode output voltage (VCM). The common-mode voltage V_{MID} sensed at node MID is fed into the OPAMP and is compared with VCM. The output of the OPAMP (node 5) controls the current drawn by transistor M3. Thus, transistor M4 outputs a fixed bias current (ratioed from IB) and the common-mode voltage V_{MID} is changed by varying exactly how much current transistor M3 is drawing. If it is desired to raise the common-mode voltage of the output, the amount of current drawn by transistor M3 is decreased. The OPAMP senses the difference - up or down - between the actual common-mode voltage V_{MID} as sensed at node MID and the desired common-mode voltage VCM, and drives transistor M3 to control the output common-mode voltage to compensate for the difference.

[0006] Many factors are considered in designing integrated circuits including the physical size, the temperature characteristics and the power requirements of the components that make up the IC. A very simple operational amplifier generally comprises at least 5 - 7 transistors. Further, a high-gain OPAMP can oscillate, causing instability or improper operation of the circuit. To insure stability the OPAMP must be compensated which results in delayed correction of the common-mode output voltage due to changes in the common-mode voltage at MID. This delay may temporarily result in the output common-mode voltage not falling within the desired range. Thus, it would be desirable to simplify the common-mode control by reducing the number of components required, decreasing the power and temperature factors, and still provide stable control of the common-mode voltage.

Summary of the Present Invention

[0007] It is therefore an object of the present invention to provide an improved method and device for controlling the output common-mode voltage of a differential buffer.

[0008] It is another object of the present invention to provide an improved method and device for controlling the output common-mode of a differential buffer using a reduced number of components and having decreased power, size, and temperature factors.

[0009] It is also an object of the present invention to provide a device (or an integrated circuit including a device) for controlling the common-mode output voltage of a differential buffer to a desired value, comprising a first current source providing a first current to the output of said differential buffer; a second current source providing a second current to the output of said differential buffer, said second current being opposite in polarity and lower in magnitude than said first bias current; sensing means for sensing the common-mode output voltage of said differential amplifier and providing an adjustment current at a node of said sensing means; and adding means for adding said adjustment current to said second current to adjust the common-mode output voltage to said desired value.

[0010] It is a further object of the present invention to

provide a method of controlling the common-mode output voltage of a differential buffer to a desired value, comprising the steps of supplying a first current to the output of said differential buffer; supplying a second current to the output of said differential buffer, said second current being opposite in polarity and lower in magnitude than said first current; sensing the common-mode output voltage of said differential buffer and providing an adjustment current at a node of said sensing means; and adding said adjustment current to said second current to adjust the common-mode output voltage to said desired value.

Brief Description of the Drawings

[0011]

Figure 1 is schematic drawing of a prior art LVDS buffer circuit;
Figure 2 is a schematic drawing of a first embodiment of a common-mode output voltage control circuit according to the present invention;
Figure 3 is a schematic drawing of a second embodiment of a common-mode output voltage control circuit according to the present invention;
Figure 4 is a schematic drawing of a third embodiment of a common-mode output voltage control circuit according to the present invention; and
Figure 5 is a schematic drawing of a fourth embodiment of a common-mode output voltage control circuit according to the present invention.

Detailed Descriptions of the Preferred Embodiments

[0012] In Fig. 2, a first embodiment of the present invention is shown with an LVDS output buffer in which the OPAMP of Fig. 1 is removed. As with the prior art circuit, transistors MB and M4 comprise a positive current source and supply current into node 4. Transistor M3 is still drawing current away from node 3 and thus the common-mode voltage is still controlled by varying the current drawn by transistor M3.

[0013] In this circuit, however, the current in transistor M3 is varied without using an OPAMP. The bias current (IB) flowing in transistor MB still develops a ratioed current in M4. However, a transistor MBX on the IB bias rail sends a "copy" of MB's current into node 5, where it flows through diode connected transistor M3B. Since transistor M3 shares the node 5 bias rail with M3B, M3 draws a current from node 3 that is ratioed to the input bias current IB. The combination of transistors MBX, M3B, and M3 form a negative current source. However, the value of the current drawn by this negative current source is deliberately selected to be smaller than the current supplied by the positive current source comprising transistors MB and M4. The W/L ratio of transistors M3B and M3 are selected to create a current in transistor M3 which is approximately 70% of the current flowing in transistor M4. By way of example only, if the W/L ratios of transistors MBX, M4, M3B, and M3 are selected to be 25/0.7; 12x25/0.7; 36/0.6; and 10x30/0.6, respectively, an appropriate ratio is achieved.

[0014] With this variance in current between transistors M3 and M4, the common-mode voltage V_{MID} would increase up to the positive rail (V_{DDB}). To avoid this, transistor M3CM, a P-channel transistor, is placed in a common-gate configuration between the common-mode sense point mode MID and node 5 to provide negative feedback which, in turn, controls the output common-mode voltage.

[0015] P-channel transistor M3CM is placed with its source and bulk nodes connected to node MID, the gate grounded and the drain connected to node 5. The bulk node could also be connected to V_{DDB}. In this configuration, current flows from node MID into the diode connected transistor M3B when the voltage V_{MID} is greater than $\approx V_t$ (V_t is the threshold voltage of transistor M3B) which in this technology is $\approx$ 1V. With transistor M3CM's gate grounded, the output common-mode voltage V_{MID} is set at approximately 1 volt (the approximate V_{GS} of a P-channel device). Since the gate of transistor M3CM is grounded, if the voltage at node MID goes above 1 volt, current will start to flow down from node MID through transistor M3CM to node 5 and into transistor M3B. The current flows through transistor M3B on its way to ground and, since transistor M3B is receiving more current than before (the current being provided by transistor M3CM), the V_{GS} of M3 is increased, thereby increasing the current drawn out of node 3 by transistor M3. When this additional current flows through transistor M3B it in turn increases the current in transistor M3 which in turn lowers the output common-mode voltage. Thus, transistors M3CM, MBX, M3B and M3 combine to provide the negative feedback as did the OPAMP in the prior art circuit.

[0016] To summarize, as V_{MID} rises upwards, current flows through transistor M3CM into node 5, increasing the current drawn by transistor M3, thereby reducing V_{MID} back down to the desired level (1 volt in this example).

[0017] Transistors MBX, M3B and M3CM, configured as shown in Fig. 2, provide means for increasing the V_{GS} of M3 when V_{MID} increases. The V_{GS} of M3 will rise in correspondence to a rise in V_{MID} due to the additional current flow in the impedance element (R3B or M3B) and cause V_{MID} to drop back down.

[0018] In the above example, the circuit of Fig. 2 shows a common-mode voltage output V_{MID} of approximately 1 volt. This is the normal specification for an LVDS output buffer. It is not necessary, however, to limit the common-mode voltage to 1 volt. The addition of two transistors to the circuit of Figure 2 allows the common-mode to be set to any voltage between approximately (GNDB +1 volt) and (V_{DDB} -1 volt). Referring to Figure 3, instead of connecting the gate of M3CM to ground, it

is instead connected to a variable voltage developed at node 6. Transistor M3LS is a diode-connected P-channel device having its gate connected to node 6 and a desired common mode voltage VCM is connected to the source and bulk nodes of transistor M3LS. N-channel transistor M3I has its drain connected to the drain of M3LS and to node 6, and its source and bulk node are connected to ground. The gate of transistor M3I is connected to the gate of M3B. Thus, if the amount of current flowing through M3B changes, it will also change the current in M3I. M3I is sized such that its current is equal to or ratioed to the average current flowing in M3CM during normal operation. The current that M3I pulls through diode-connected transistor M3LS creates a V_{GS} of M3LS which is equal to the nominal V_{GS} of M3CM. The size of M3I is nominally one-third the size of M3B. Thus, diode connected P-channel M3LS provides at node 6 a level-shifted version (e.g., VCM reduced by the V_{GS} of transistor M3LS) of the desired common-mode operating voltage VCM. Node 6 then is used to drive the gate of M3CM. Since the V_{GS} drop of M3LS and M3CM should be about equal, V_{MID} is effectively set to the VCM value. This circuit displays output common-mode regulation equivalent to the circuit of Figure 2.

[0019] Transistors M3I and M3LS are ratioed to match transistors M3CM and M3. They do not need to be equal, e.g., transistors M3I and M3LS can be several times smaller than transistors M3CM and M3.

[0020] Once the circuit is configured as shown in Figure 3, the current flowing through transistor M3LS is scaled to transistor M3CM such that transistor M3CM experiences the same V_{GS} as transistor M3LS. Even though each one may be handling a different amount of current, transistors M3LS and M3CM are ratioed so that this equivalency of V_{GS} exists. Transistor M3CM still transfers current from node MID into node 5, providing the negative feedback which controls the common-mode voltage. Transistors M3LS and M3I create a level-shifted version of VCM. Transistor M3LS is level-shifting the voltage from the desired common-mode voltage (VCM) down to the gate potential on M3CM that will be needed to make V_{MID} equal to VCM. Transistor M3LS is level-shifting from VCM down to node 6 and transistor M3CM, in a sense, level-shifts up from node 6 to node MID by the same amount as the shift down, making VCM and V_{MID} approximately the same.

[0021] As an example, if we assume that VCM is approximately two volts, node 6 will assume a voltage of approximately one volt because it takes about one volt to turn transistor M3LS on. Given that node 6 is ≈ 1V, V_{MID} will equal 1V plus the V_{GS} of M3CM, or 2V. In other words, VCM is shifted down by the V_{GS} of M3LS at node 6 and then shifted back up by the V_{GS} of M3CM, resulting in V_{MID} being approximately equal to VCM.

[0022] As the current flow through M3CM varies, to adjust the common mode voltage, that current also flows through M3B which, in turn, varies the current through M3I. This in turn varies the current flowing through transistor M3LS. Thus, as more current flows through M3CM, more current also flows through M3LS, and thus the $V_{GS's}$ of M3CM and M3LS change in the same sense and by about the same amount. This keeps VCM equal to V_{MID} and allows the selection of a VCM voltage anywhere from approximately 1 to 4 volts if running from a 5 volt supply.

[0023] Figure 4 shows an alternative embodiment to the circuit of Fig. 2. In Fig. 4, transistor MBX is removed and resistor R3B replaces transistor M3B. The function of resistor R3B is the same of that of transistor M3B, i. e., resistor R3B introduces an impedance at the controlling node of transistor M3, thereby increasing the magnitude of the current in transistor M3 which in turn lowers the output common-mode voltage of the differential buffer. This embodiment is more process sensitive than the previous embodiments (e.g., there is more output common-mode voltage variation with changes in temperature, power supply voltage, and processing).

[0024] Alternatively, Fig. 5 shows another alternative to the circuit of Fig. 2. In this circuit, transistors M3CM and M3B are replaced by resistors R3CM and R3B, respectively. This allows a designer to select a resistor ratio of R3CM to R3B to set the common-mode output voltage over a wide range of voltages. The circuit of Fig. 5, having fixed resistances R3CM and R3B, will not have the flexibility of the circuit of Fig. 3, since once the resistor ratio R3CM to R3B is selected, it cannot be changed. This configuration, however, still allows flexibility in selection of the desired, common-mode output voltage. Further, the resistor ratios could be mask programmable by changing metal routing. Alternatively, one or both resistors R3CM and R3B could comprise series or parallel resistor combinations. Individual resistor contributions to the equivalent resistances could then be controlled by including transistors as switching elements. Thus, digital signals could control the ratio or R3CM to R3B.

[0025] In circuit simulation of the Fig. 5 circuit conducted by the applicant, this embodiment demonstrated equal or marginally better performance than the circuit of Fig. 2, with respect to output common-mode voltage variation changes in temperature, power supply voltage, and processing.

[0026] Having thus described a few particular embodiments of the invention, various alterations, modifications, and improvements will readily occur to those skilled in the art. For example, the circuits presented could also be implemented by fixing the current n M3B and allowing the current in M4 to be adjusted. This could be accomplished by exchanging the N and P transistors of Fig. 2 and swapping the power supply connections. Further, the circuits could be constructed in a bipolar implementation. Such alterations, modifications and improvements as are made obvious by this disclosure are intended to be part of this description though not expressly stated herein, and are intended to be within the spirit and scope of the invention. The foregoing descrip-

tion is by way of example only; and not limiting. The invention is limited only as defined in the following claims and equivalents thereto.

Claims

1. A device for controlling the common-mode output voltage of a differential buffer to a desired value, comprising:

   a first current source providing a first current to the output of said differential buffer;
   a second current source providing a second current to the output of said differential buffer, said second current being opposite in polarity and lower in magnitude than said first current;
   sensing means for sensing the common-mode output voltage of said differential buffer and providing an adjustment current at a node of said sensing means; and
   adding means for adding said adjustment current to said second current to adjust the common-mode output voltage to said desired value.

2. An integrated circuit including a device for controlling the common-mode output voltage of a differential buffer to a desired value, comprising:

   a first current source providing a first current to the output of said differential buffer;
   a second current source providing a second current to the output of said differential buffer, said second current being opposite in polarity and lower in magnitude than said first current;
   sensing means for sensing the common-mode output voltage of said differential buffer and providing an adjustment current at a node of said sensing means; and
   adding means for adding said adjustment current to said second current to adjust the common-mode output voltage to said desired value.

3. A device as claimed in claim 1, or an integrated circuit as claimed in claim 2, wherein said adding means comprises a first transistor connected between said sensing means and said second current source.

4. A device as claimed in claim 1, or an integrated circuit as claimed in claim 2, wherein said adding means comprises a resistance device connected between said sensing means and said second current source.

5. A device or integrated circuit as claimed in claim 3, wherein said first transistor has its source and bulk node connected to said node of said sensing means, its drain connected to said second current source, and its gate connected to ground.

6. A device or integrated circuit as claimed in claim 3, wherein said first transistor is a P-channel transistor.

7. A device or integrated circuit as claimed in claim 3, wherein said second current source comprises an impedance device connected between the drain of said first transistor and ground, and a second transistor connected in a common-source configuration and having its gate connected to the drain of said first transistor.

8. A device or integrated circuit as claimed in claim 4, wherein said second current source comprises an impedance device connected between said resistance device and ground, and a second transistor connected in a common-source configuration and having its gate connected to the drain of said first transistor.

9. A device or integrated circuit as claimed in claim 7 or 8, wherein said impedance device comprises resistance means.

10. A device or integrated circuit as claimed in claim 9, wherein said resistance means comprises a fixed resistor.

11. A device or integrated circuit as claimed in claim 9, wherein said resistance means comprises a variable resistance source.

12. A device or integrated circuit as claimed in claim 7 or 8, wherein said impedance device comprises a transistor.

13. A device or integrated circuit as claimed in claim 3, wherein said adding means further comprises level shifting means to adjust the gate-to-source voltage of said first transistor to a predetermined level, thereby allowing the common-mode output voltage to be controllable over a range of values.

14. A device as claimed in claim 1, or an integrated circuit as claimed in claim 2, wherein said sensing means comprises a pair of equal-valued resistors placed in series between the outputs of said differential buffer and wherein said sensing means node is located between said pair of resistors.

15. A method of controlling the common-mode output voltage of a differential buffer to a desired value, comprising the steps of:

   supplying a first current to the output of said dif-

ferential buffer;

supplying a second current to the output of said differential buffer, said second current being opposite in polarity and lower in magnitude than said first current;

sensing the common-mode output voltage of said differential buffer and providing an adjustment current at a node of said sensing means; and

adding said adjustment current to said second current to adjust the common-mode output voltage to said desired value.

FIG. 1
(PRIOR ART)

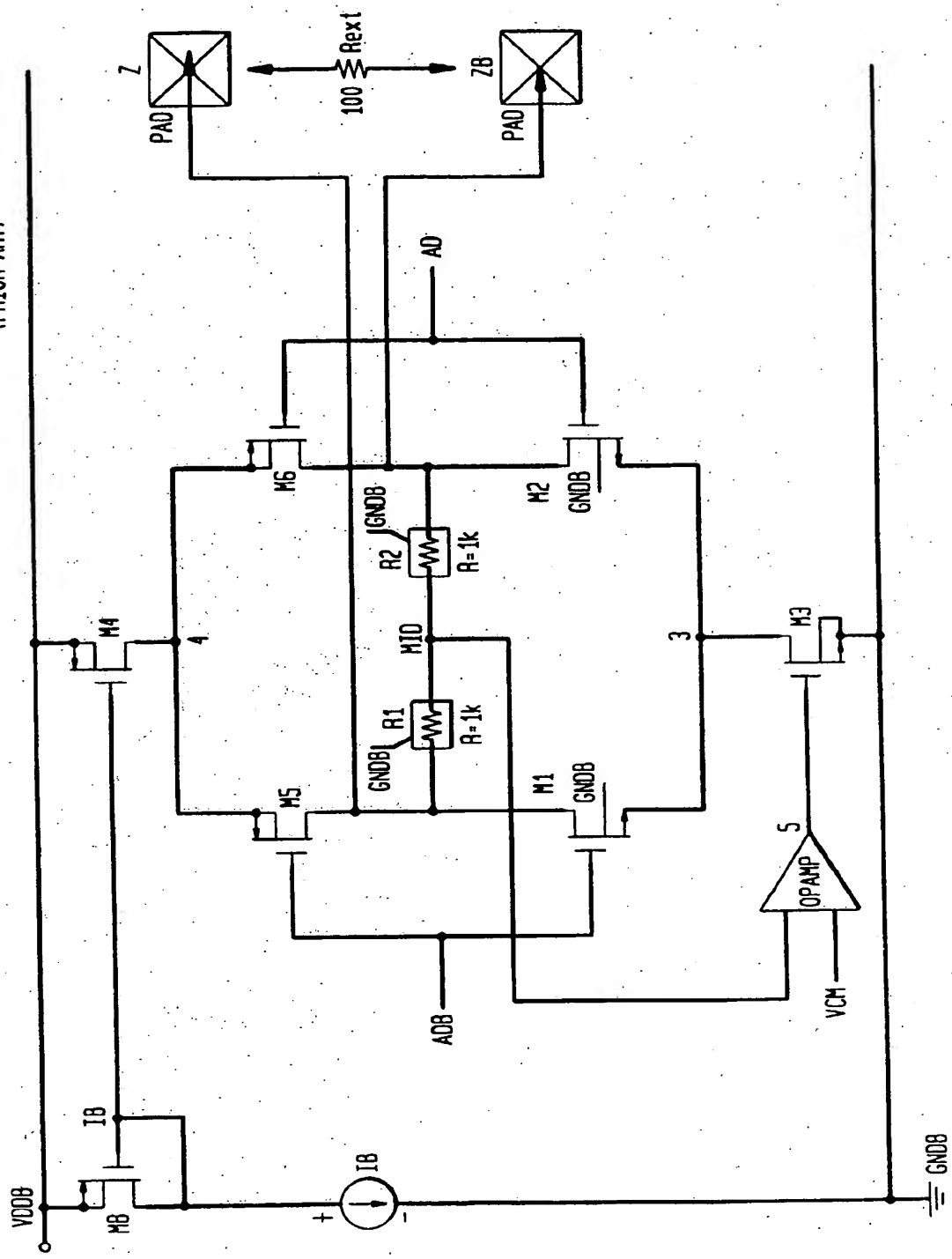

FIG. 2

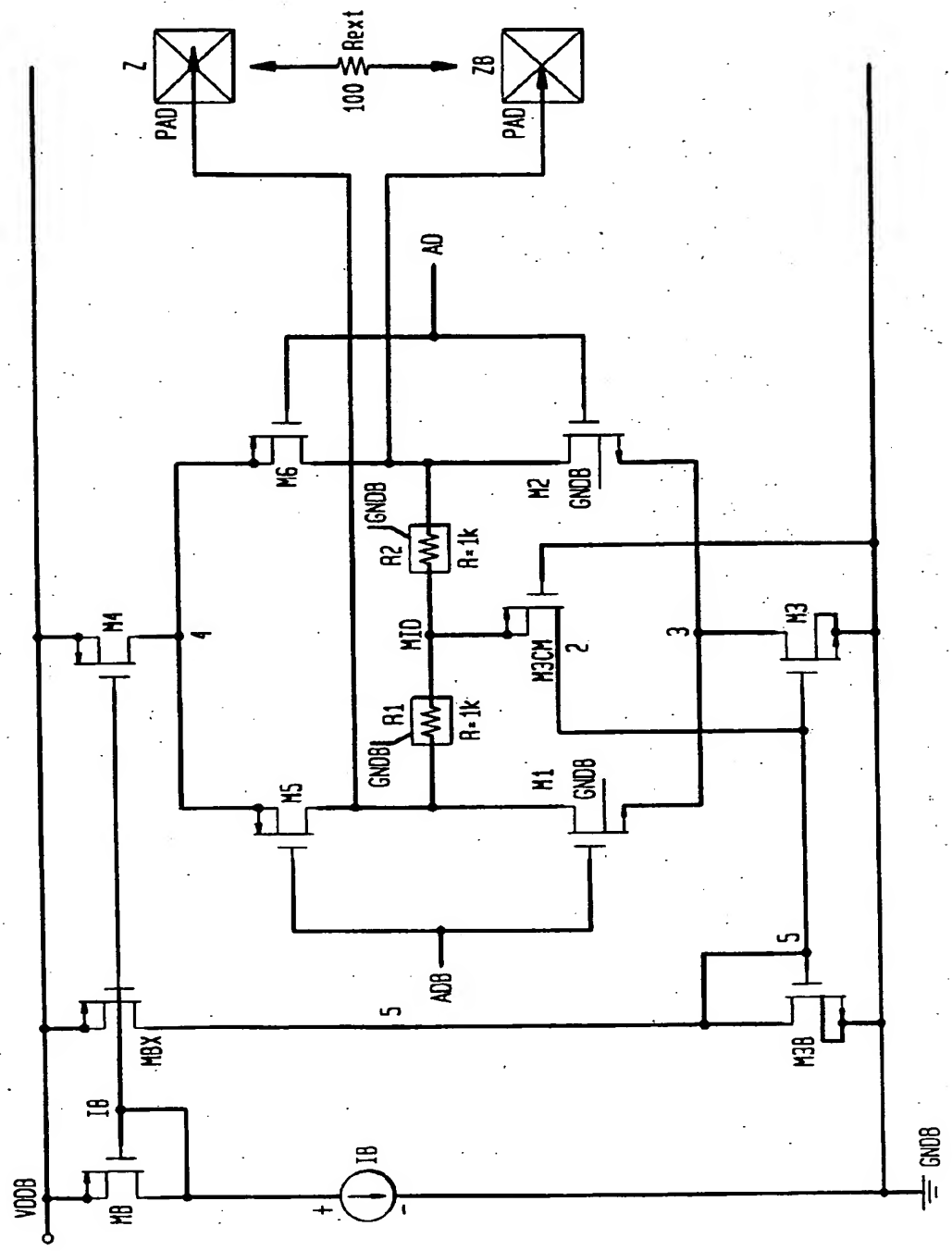
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FIG. 3

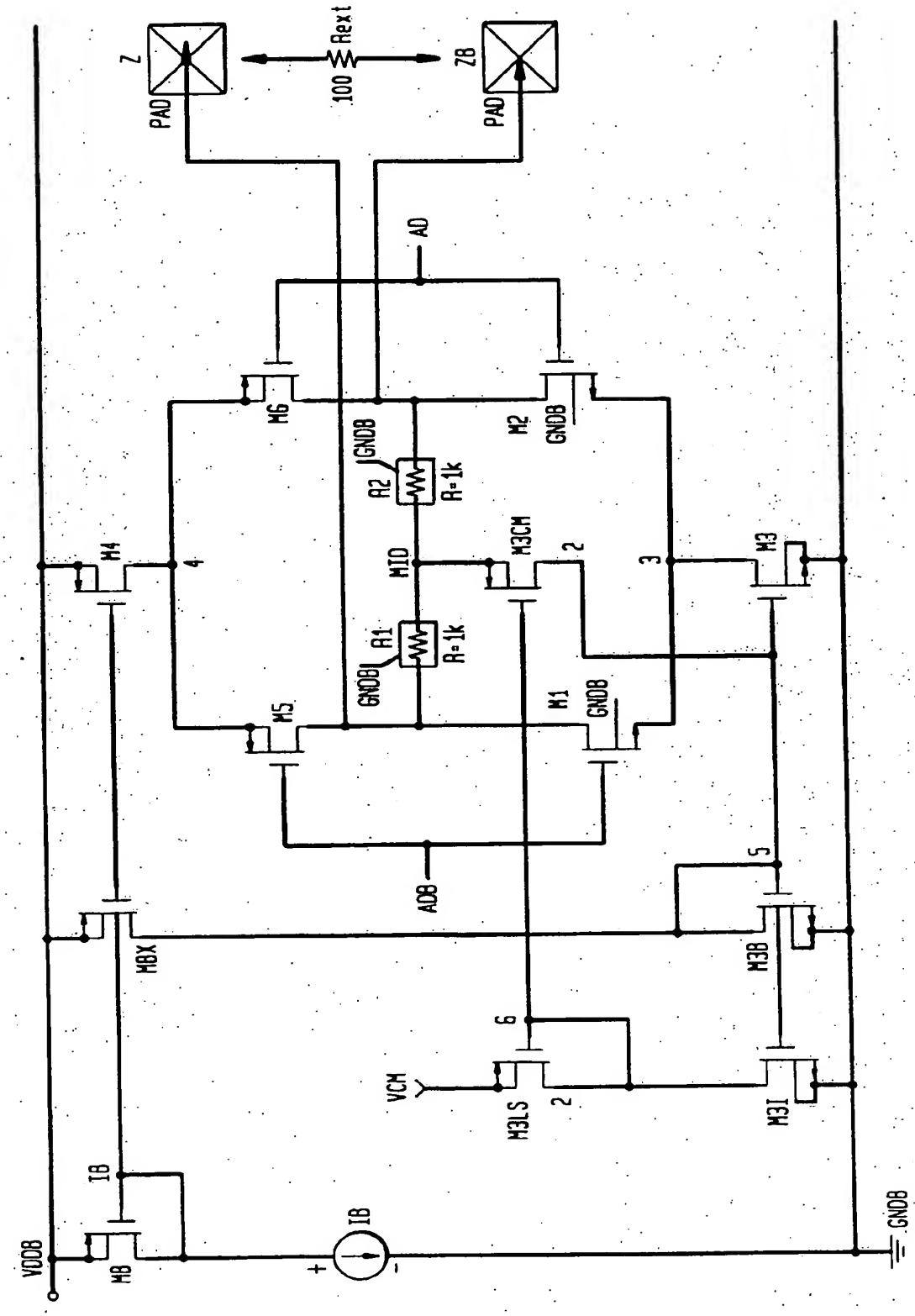
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FIG. 4

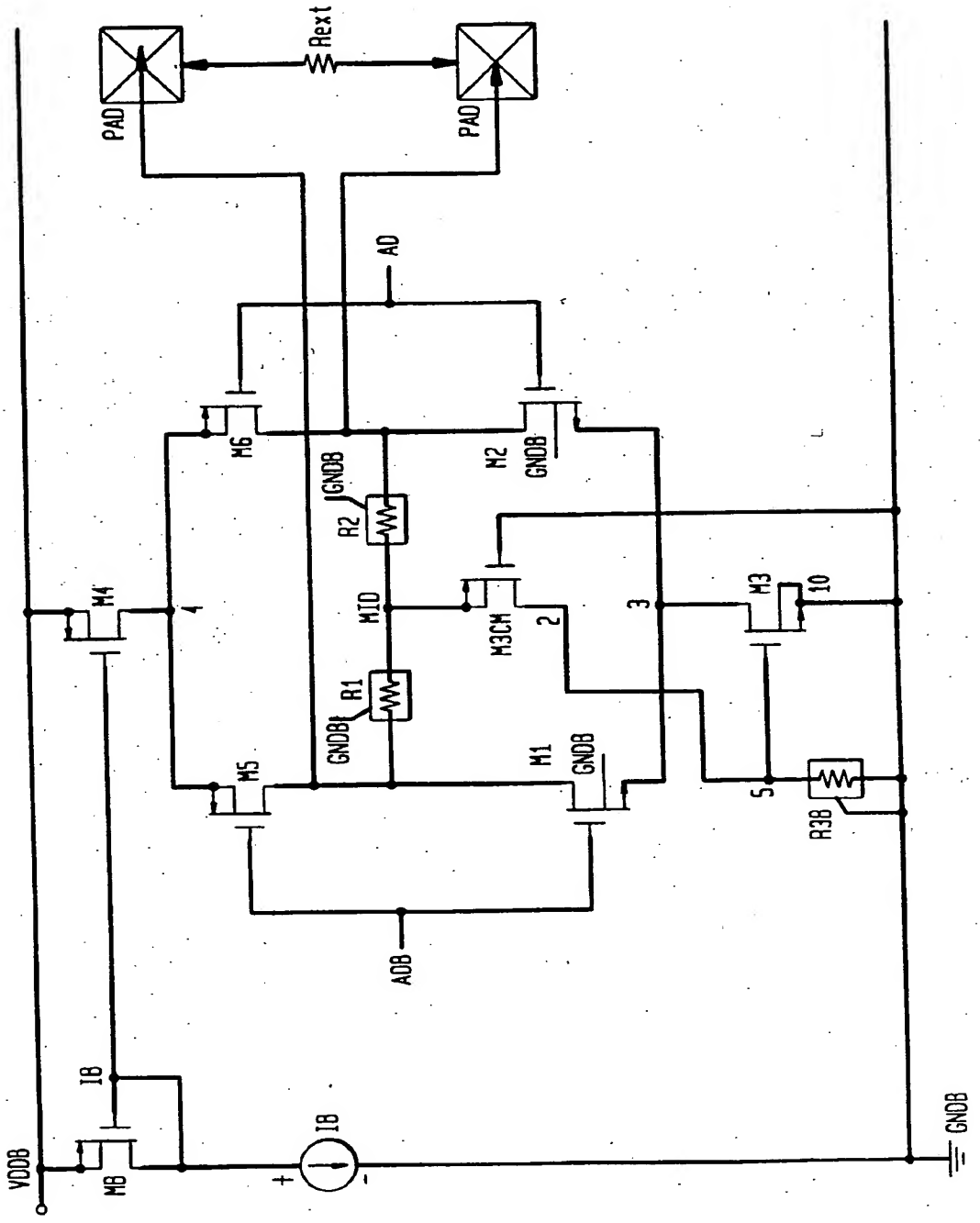
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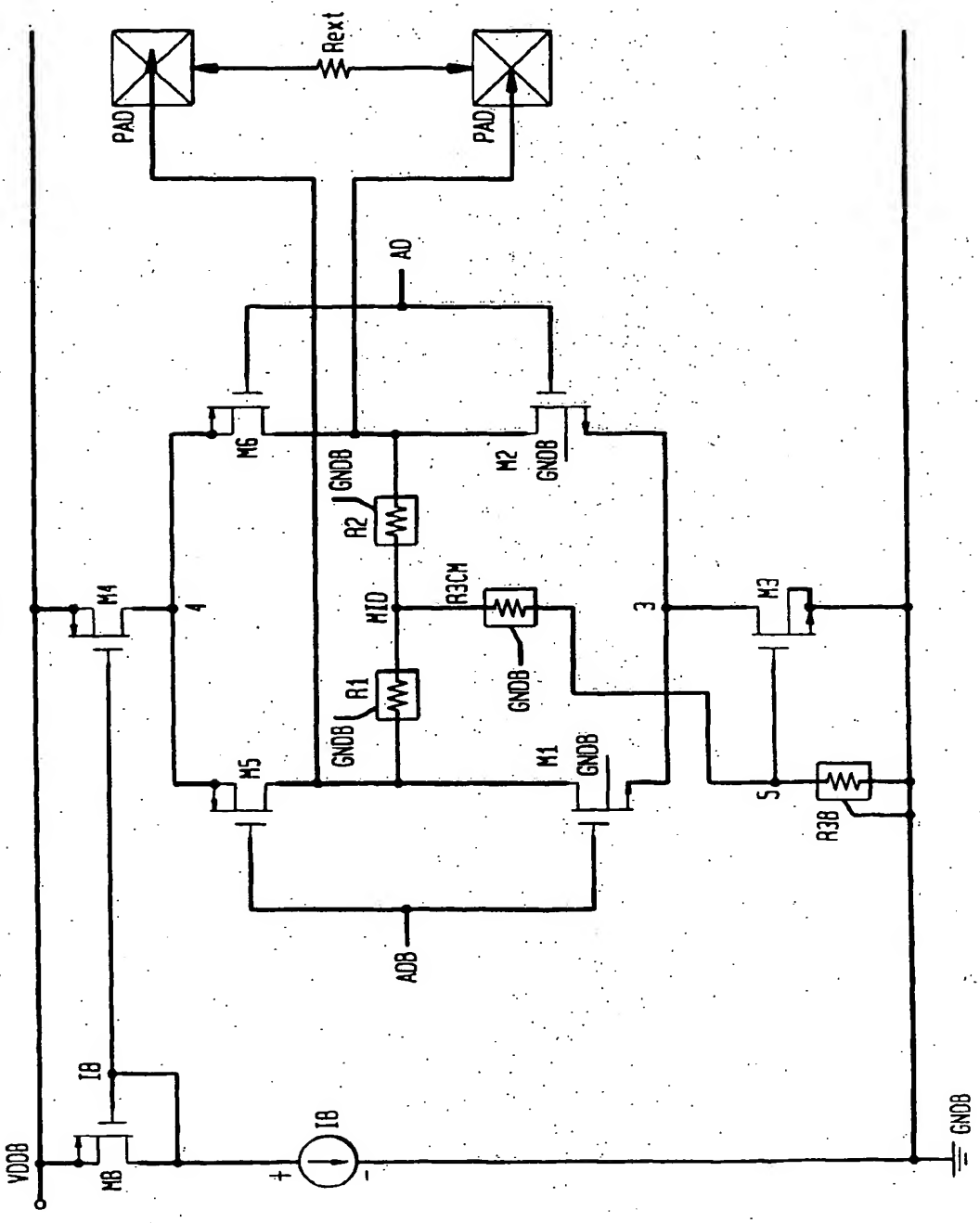
FIG. 5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EUROPEAN SEARCH REPORT

Application Number
EP 99 30 0945

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	W. CORDARO: "COMPLEMENTARY FET DIFFERENTIAL AMPLIFIER" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 16, no. 10, March 1974, pages 3227-3228, XP002103389 NEW YORK US * the whole document * ---	1,2,4, 14,15	H03F3/45
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A	US 5 703 532 A (SHIN HYUN JONG ET AL) 30 December 1997 * column 4, line 17 - column 10, line 34; figure 6 * -----	1,2,4, 14,15	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6) H03F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 May 1999	Tyberghien, G

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5703532 A	30-12-1997	NONE	

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